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	Substitute for form 1449A/PTO			Application Number	10/720,466	
	NEODMATION DIS	CI OSUBI	=	Filing Date	11/24/03	
	INFORMATION DISCLOSURE STATEMENT BY APPLICANT			First Named Inventor	Correale, Jr. et al.	
				Art Unit	2819	
	<u> </u>			Examiner Name	D. Chang	
She	et 1	of	2	Attorney Docket Number	YOR920030373US1	

U.S. PATENT DOCUMENTS						
Examiner Initials	Cite No.1	Document Number  Number - Kind Code <sup>2</sup> (# known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevan Figures Appear	
OC.	<u> </u>	US- 5594368		USAMI		
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FOREIGN PATENT DOCUMENTS									
Examiner Initials*	Cite No.1	Foreign Patent Document	Publication Date	Name of Patentee or	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T			
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Substitute for form 1449B/PTO				Complete if Known		
				Application Number (	1720 466	
INFORMATION DISCLOSURE				Filing Date	11/24/03	
STATEMENT BY APPLICANT  (use as many sheets as necessary)				First Named Inventor	Correale, Jr. et al.	
			ANI	Art Unit	2819	
				Examiner Name	D- Chang.	
Sheet	2	of	2	Attorney Docket Number	YOR920030359US1 /	

NON PATENT LITERATURE DOCUMENTS						
Examiner Initials*	Cite, No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>			
2c		LACKEY ET AL., Managing power and performance for System-on-Chip designs using Voltage Islands, Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design , 11/11/2002, Page(s) 195-202				
\$		USAMI ET AL., CLUSTERED VOLTAGE SCALING TECHNIQUES FOR LOW-POWER DESIGN, International Symposium on Low-Power Electronic Design, 4/1/1995, Page(s) 3-8, Publisher: ACM Press				
8c		USAMI ET AL., AUTOMATED LOW-POWER TECHNIQUE EXPLOITING MULTIPLE SUPPLY VOLTAGES APPLIED TO A MEDIA PROCESSOR, IEEE Journal of Solid-State Circuits, 3/1/1998, Page(s) 463-472, Volume 33, Number 3				
DC		YEH ET AL., LAYOUT TECHNIQUES SUPPORTING THE USE OF DUAL SUPPLY VOLTAGES FOR CELL-BASED DESIGNS, Proc. ACM/IEEE Design Auto. Conf., 6/1/1999, Page(s) 62-67				
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